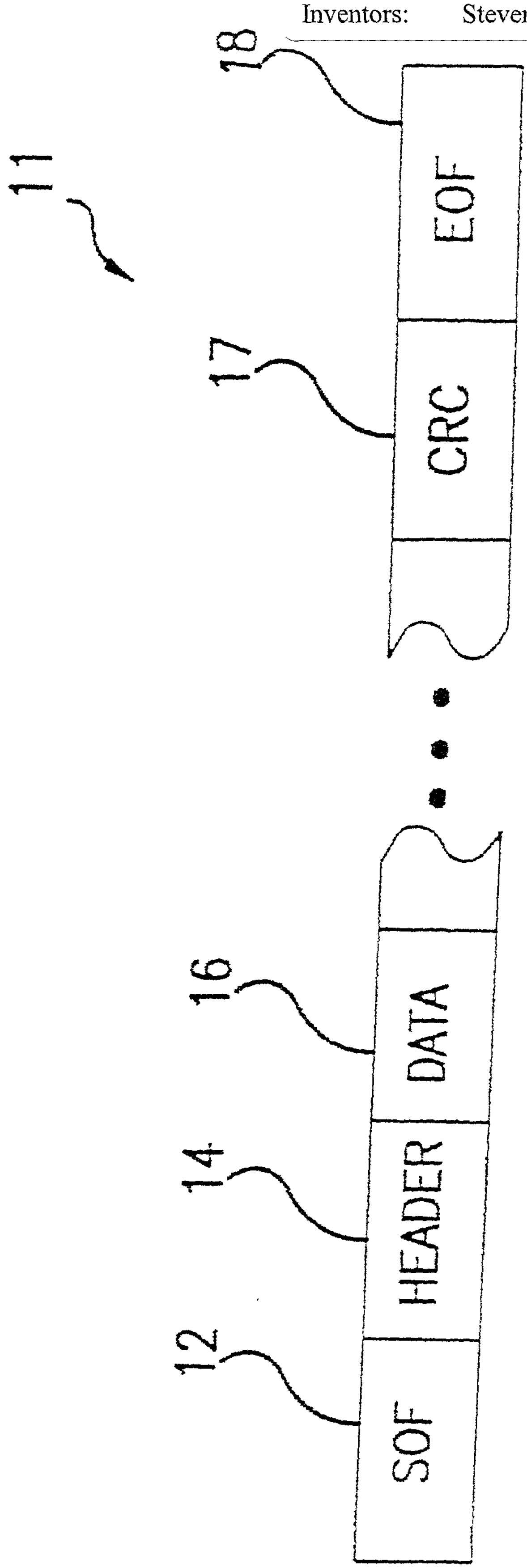

FIG. 1A
PRIOR ART

14

Routing Control (R_CTRL)	Destination ID (D_ID)	
Class Specific Control (CS_CTL)	Source ID (S_ID)	
Data Structure Type (TYPE)	Frame Control (F_CTL)	
Sequence ID (SEQ_ID)	Data Field Control (DF_CTL)	Sequence Count (SEQ_CNT)
Originator ID (OX_ID)		Responder ID (RX_ID)
Parameter or Relative Offset		

FIG. 1B
PRIOR ART

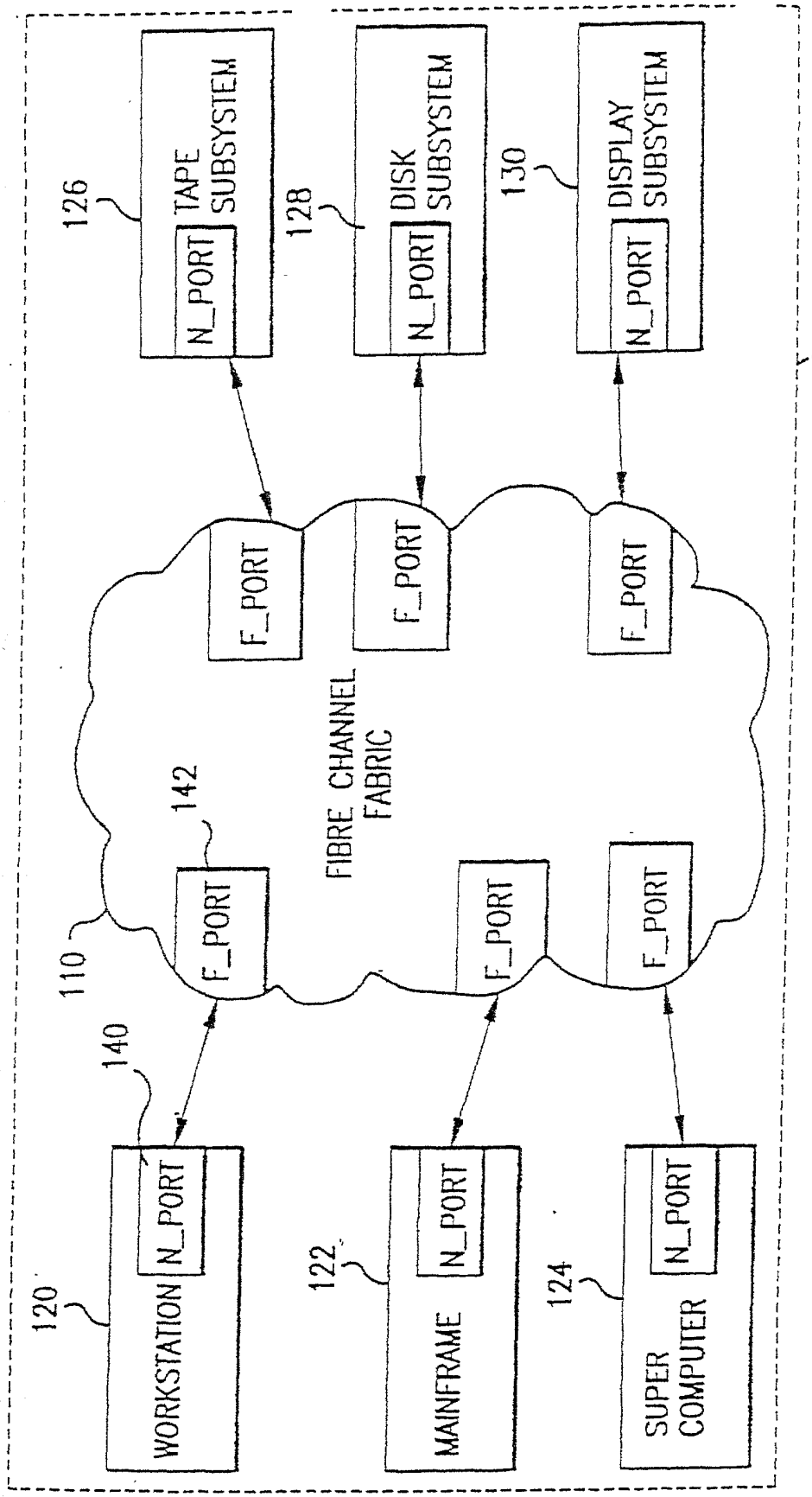

FIG. 2
PRIOR ART

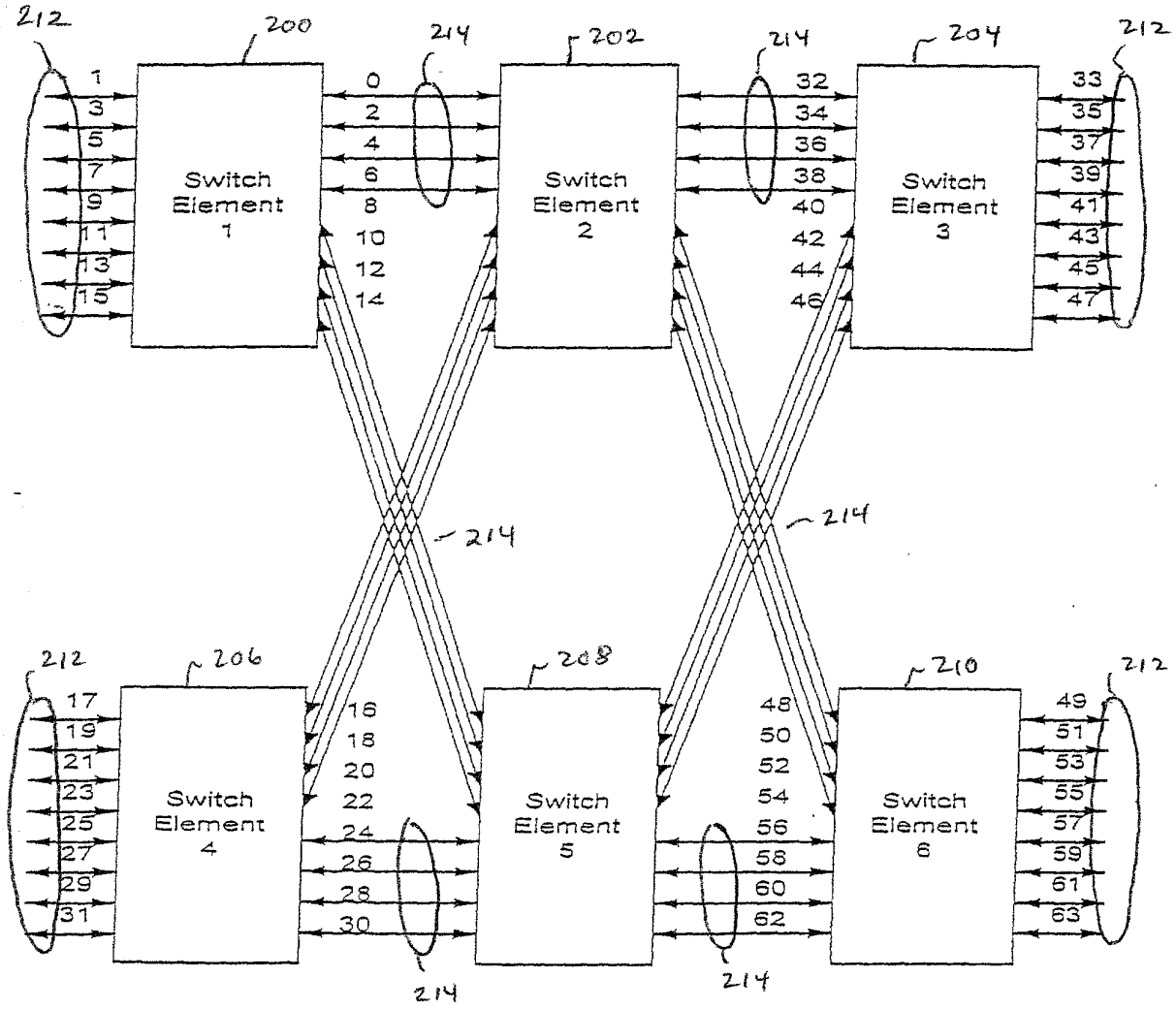

FIG. 3

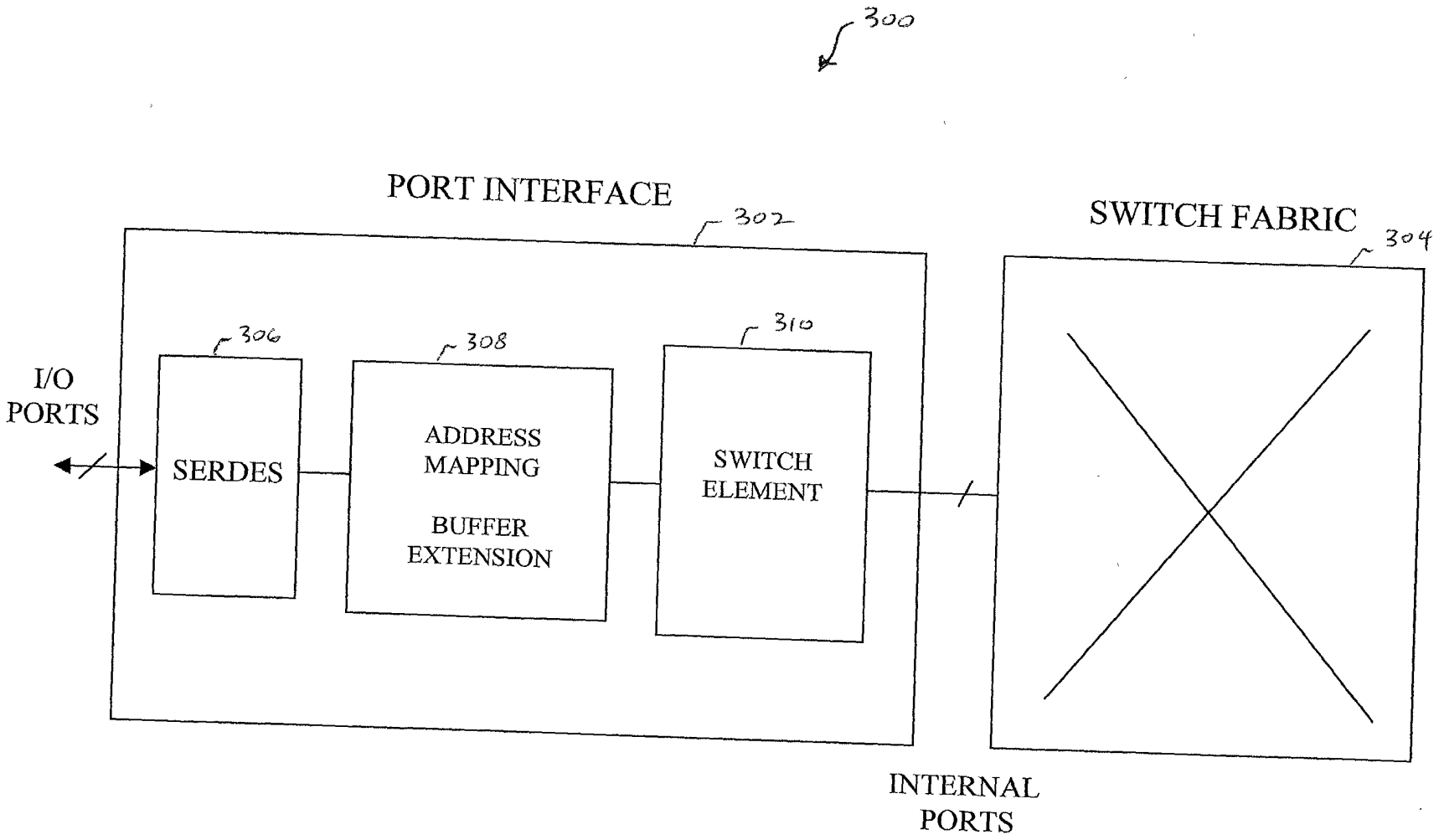

FIG. 4

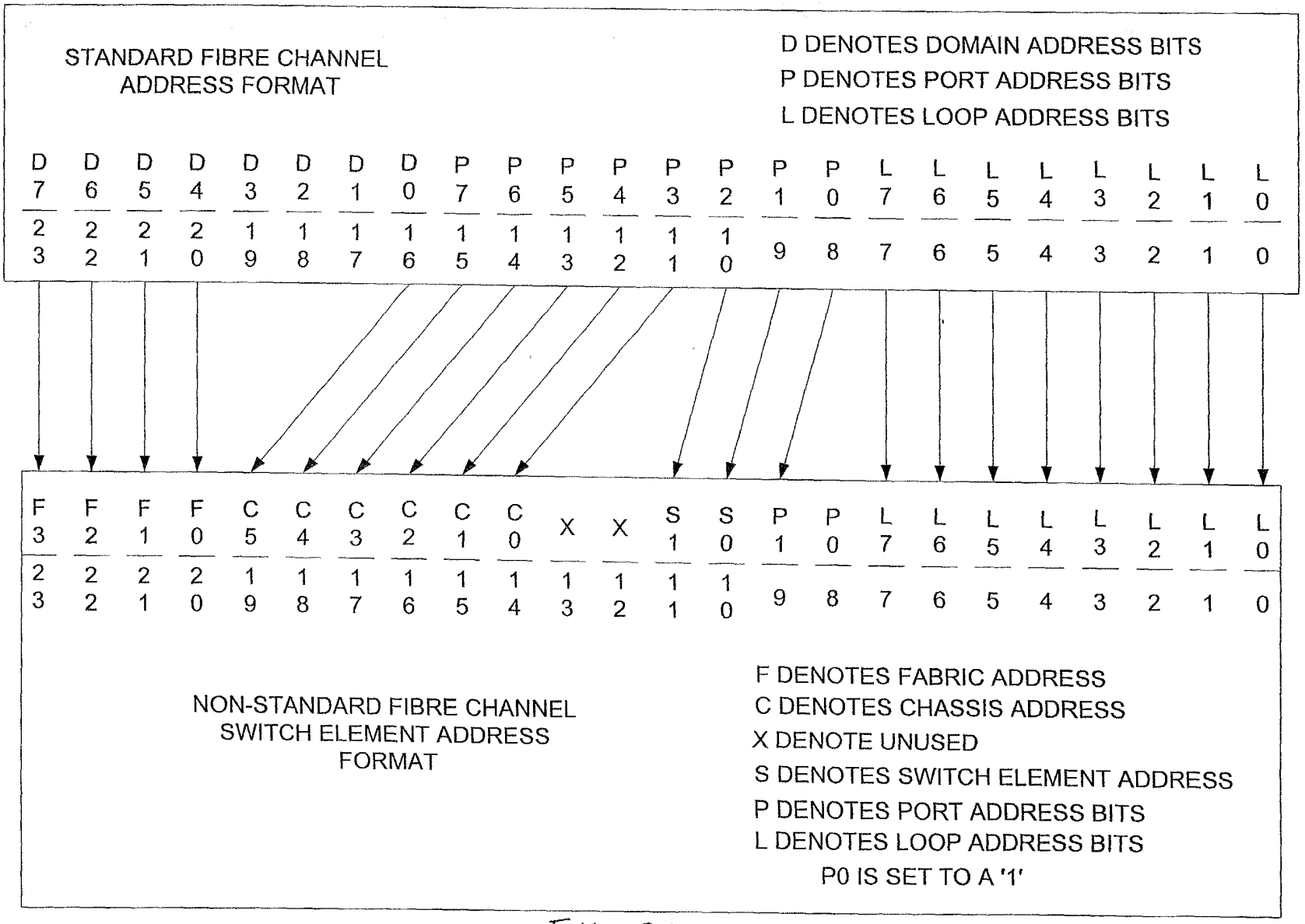

FIG. 5A

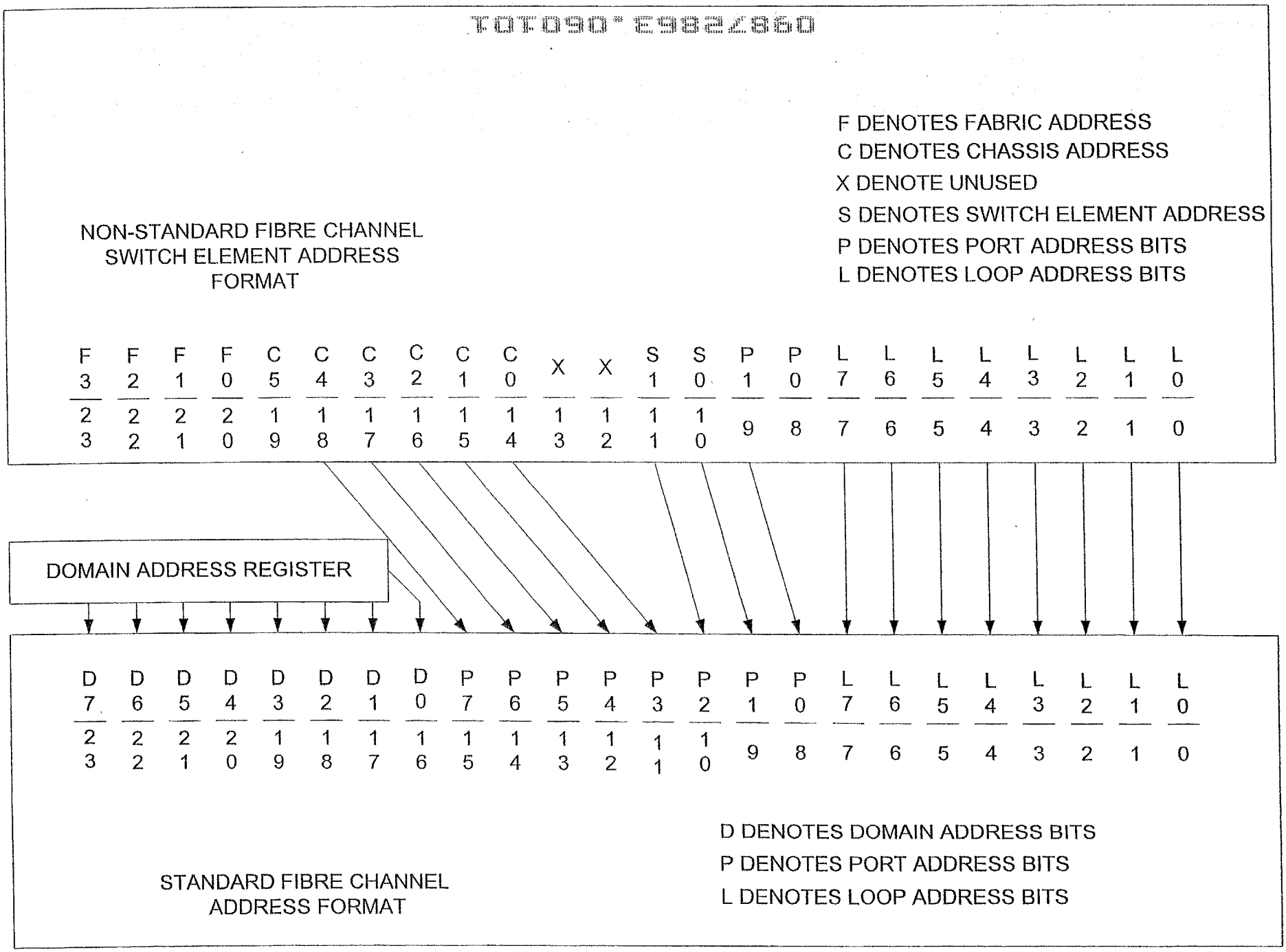

FIG. 5B

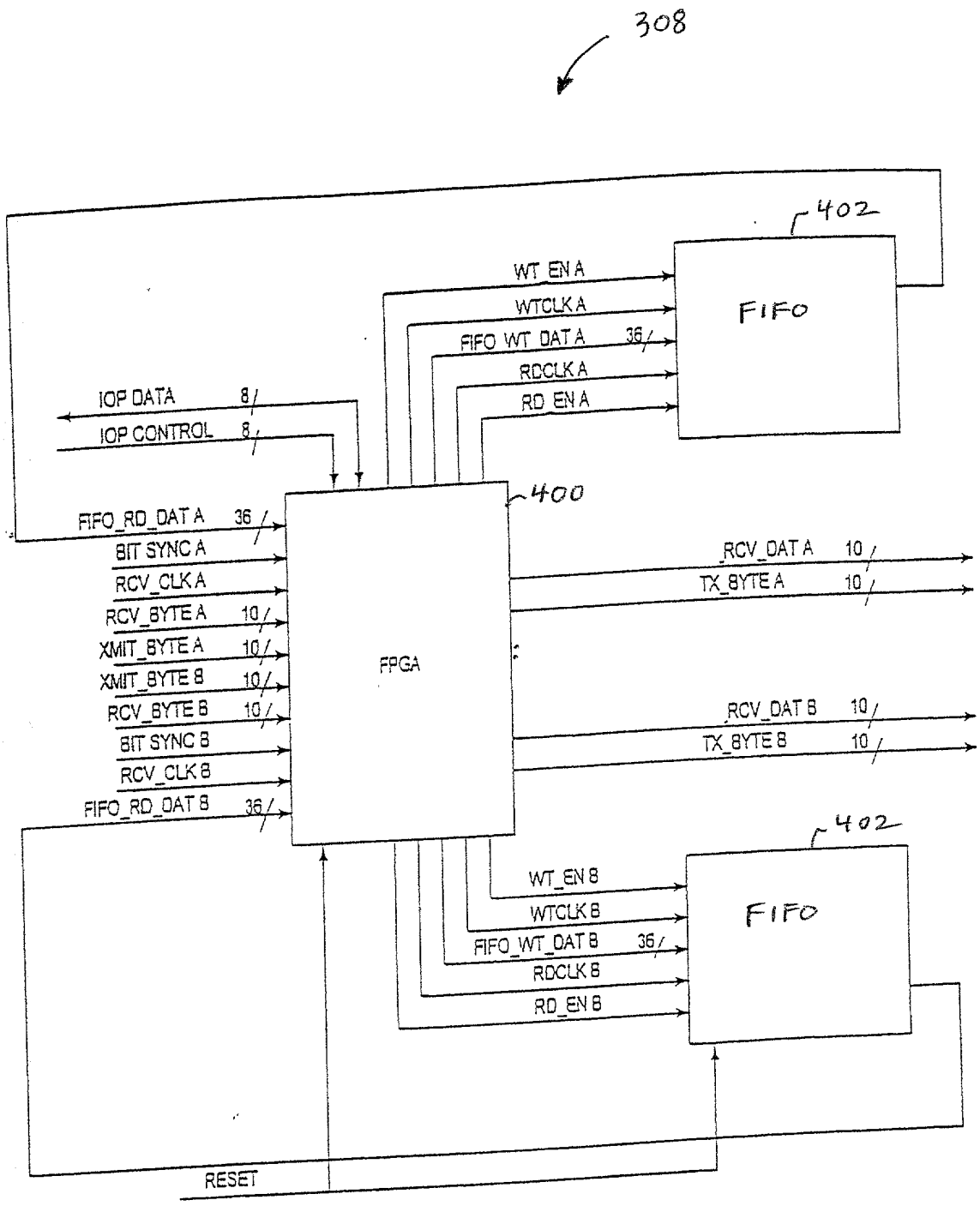
308
402
FIFO
WT_EN A
WTCLK A
FIFO_WT_DAT A
36
RDCLK A
RD_EN A
IOP DATA
8
IOP CONTROL
8
400
FIFO_RD_DAT A
36
BIT SYNC A
RCV_CLK A
RCV_BYTE A
10
XMIT_BYTE A
10
XMIT_BYTE B
10
RCV_BYTE B
10
BIT SYNC B
RCV_CLK B
FIFO_RD_DAT B
36
FPGA
RCV_DAT A
10
TX_BYTE A
10
RCV_DAT B
10
TX_BYTE B
10
402
FIFO
WT_EN B
WTCLK B
FIFO_WT_DAT B
36
RDCLK B
RD_EN B
RESET

FIG. 6

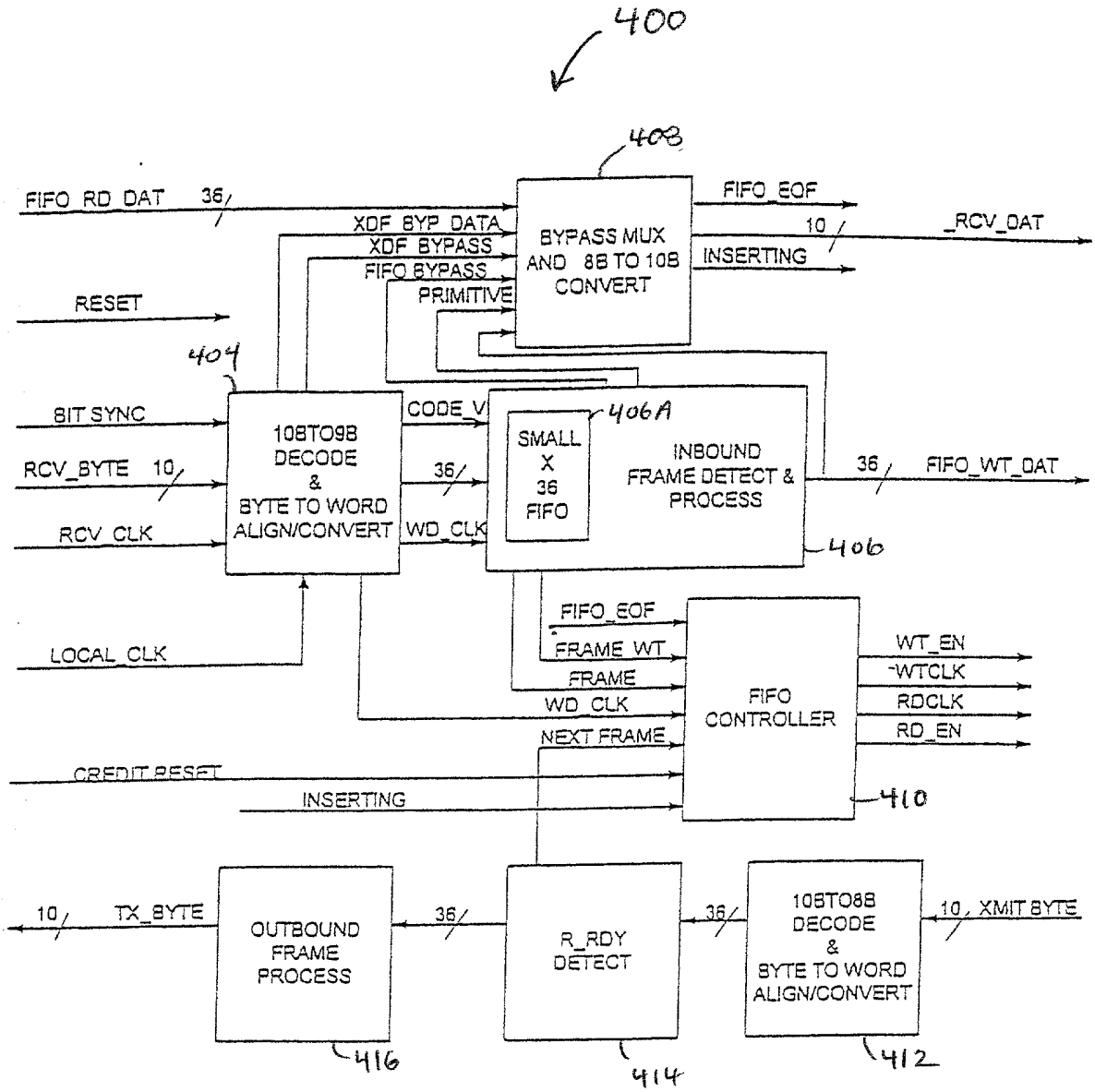
400
408
FIFO_RD_DAT
36
XDF_BYP_DATA
XDF_BYPASS
FIFO_BYPASS
PRIMITIVE
BYPASS MUX AND 8B TO 10B CONVERT
FIFO_EOF
10
_RCV_DAT
INSERTING
RESET
404
8BIT SYNC
RCV_BYTE
10
RCV_CLK
10BTO9B DECODE & BYTE TO WORD ALIGN/CONVERT
CODE_V
36
WD_CLK
406A
SMALL X 36 FIFO
INBOUND FRAME DETECT & PROCESS
36
FIFO_WT_DAT
406
LOCAL_CLK
FIFO_EOF
FRAME_WT
FRAME
WD_CLK
NEXT FRAME
FIFO CONTROLLER
WT_EN
WTCLK
RDCLK
RD_EN
CREDIT_RESET
INSERTING
410
10
TX_BYTE
OUTBOUND FRAME PROCESS
36
R_RDY DETECT
36
10BTO8B DECODE & BYTE TO WORD ALIGN/CONVERT
10
XMIT BYTE
416
414
412

FIG. 7

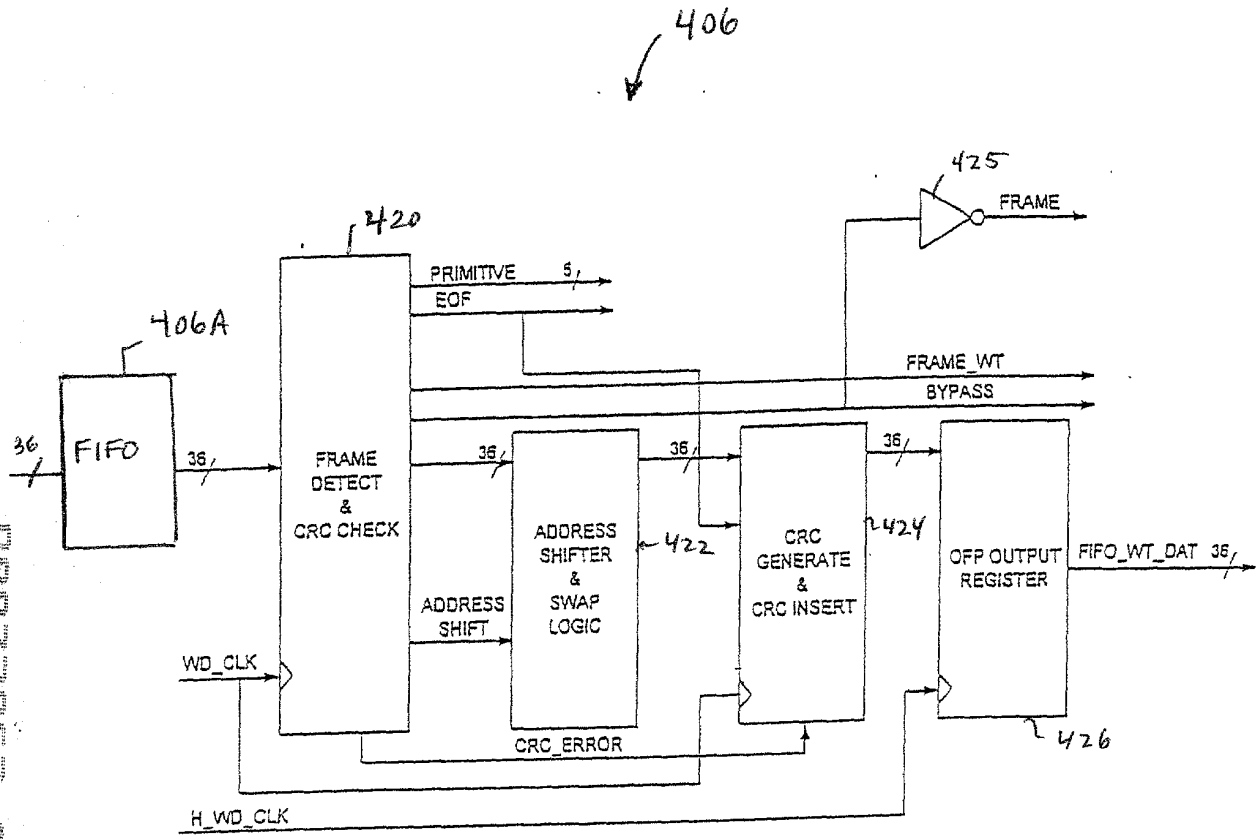
406
425
FRAME
420
PRIMITIVE
5
EOF
406A
FRAME_WT
BYPASS
36
FIFO
36
FRAME
DETECT
&
CRC CHECK
36
36
ADDRESS
SHIFTER
&
SWAP
LOGIC
422
36
CRC
GENERATE
&
CRC INSERT
424
36
OFP OUTPUT
REGISTER
FIFO_WT_DAT
36
ADDRESS
SHIFT
WD_CLK
CRC_ERROR
426
H_WD_CLK

FIG. 8

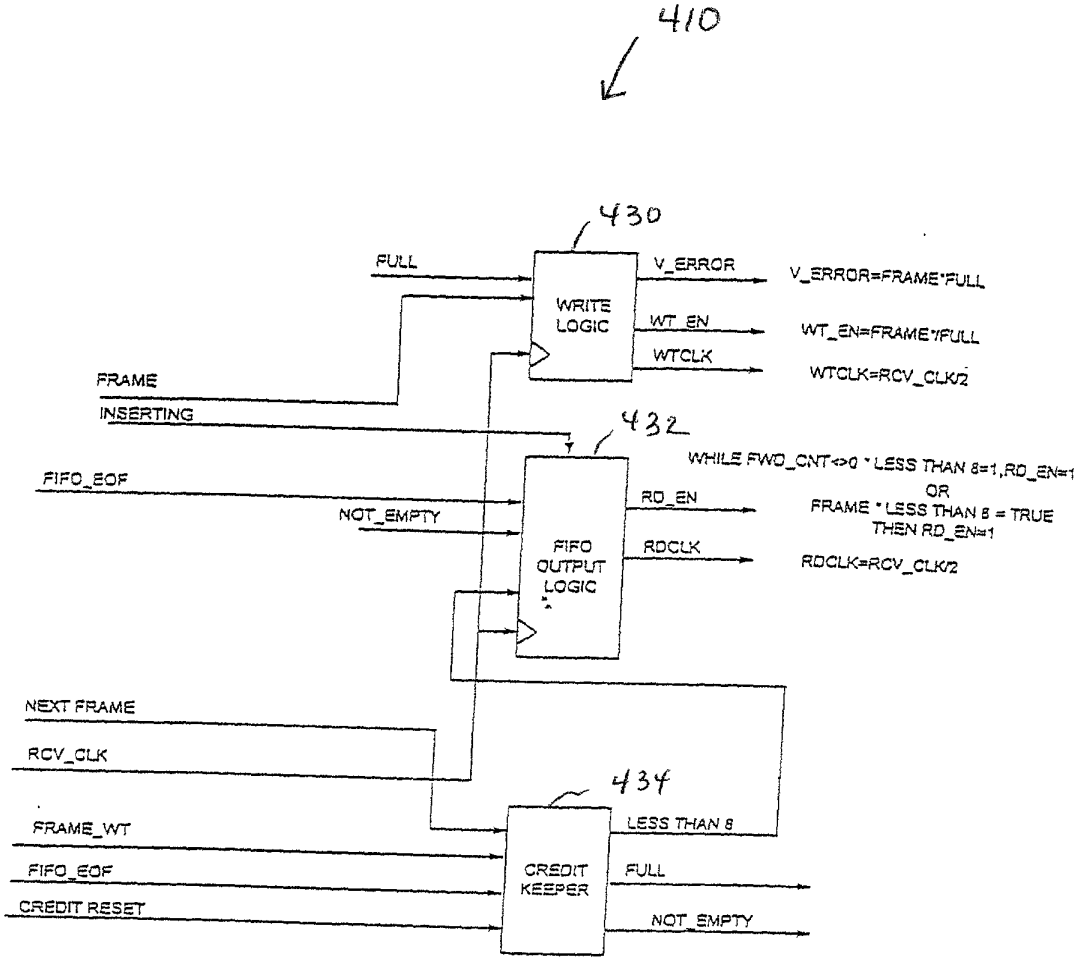

FIG. 9

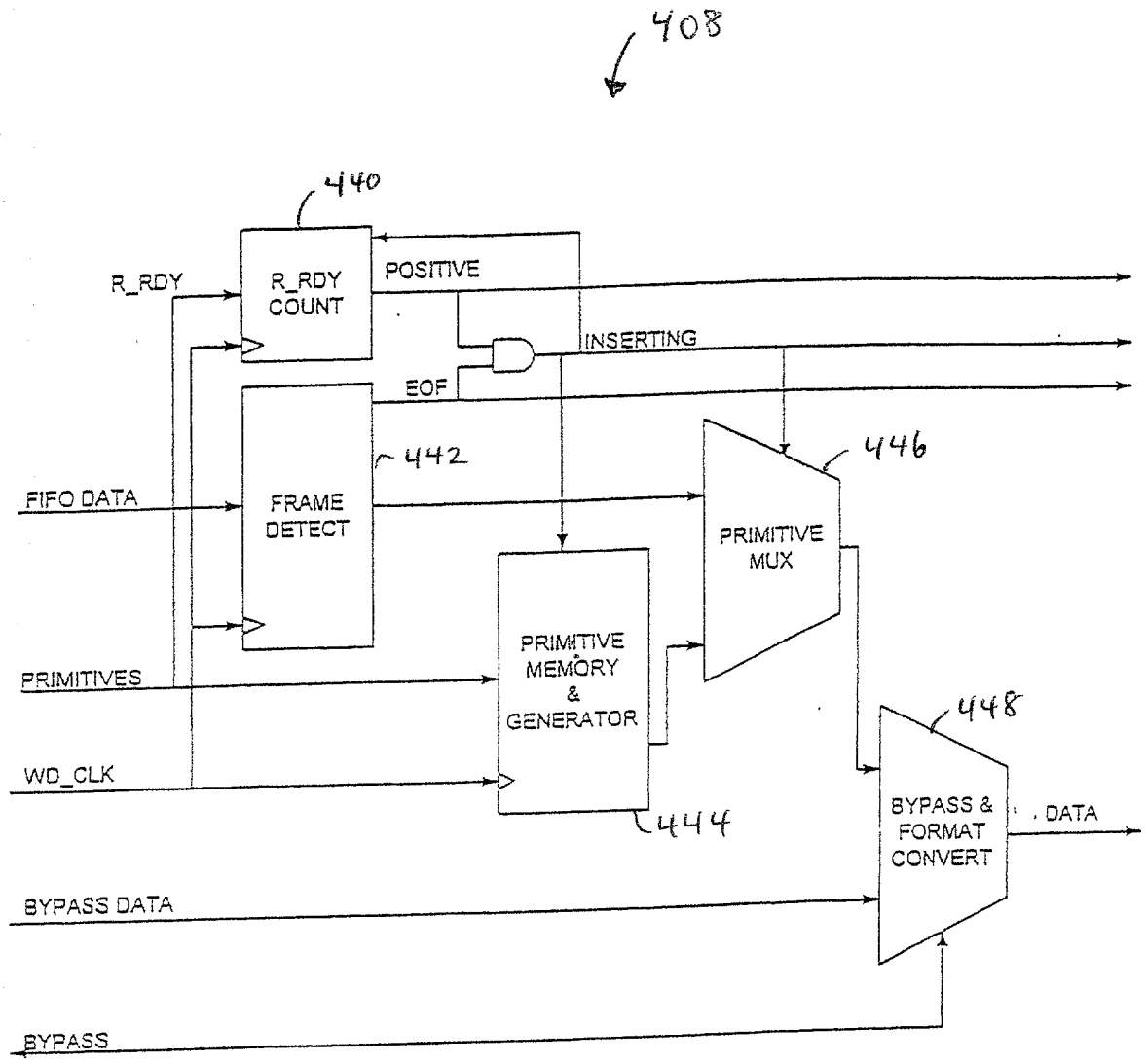
408
440
R_RDY
R_RDY COUNT
POSITIVE
INSERTING
EOF
442
FIFO DATA
FRAME DETECT
446
PRIMITIVE MUX
PRIMITIVES
PRIMITIVE MEMORY & GENERATOR
448
WD_CLK
444
BYPASS & FORMAT CONVERT
DATA
BYPASS DATA
BYPASS

FIG. 10

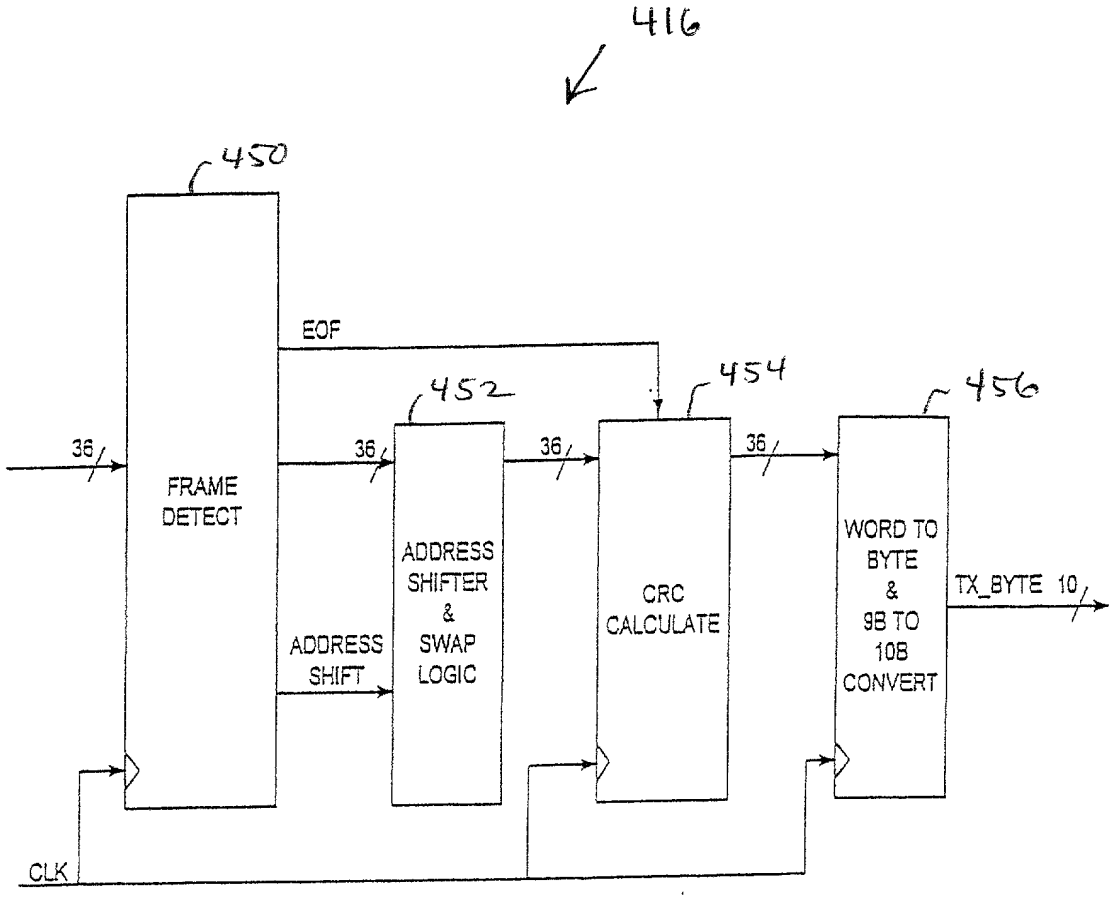

FIG. 11

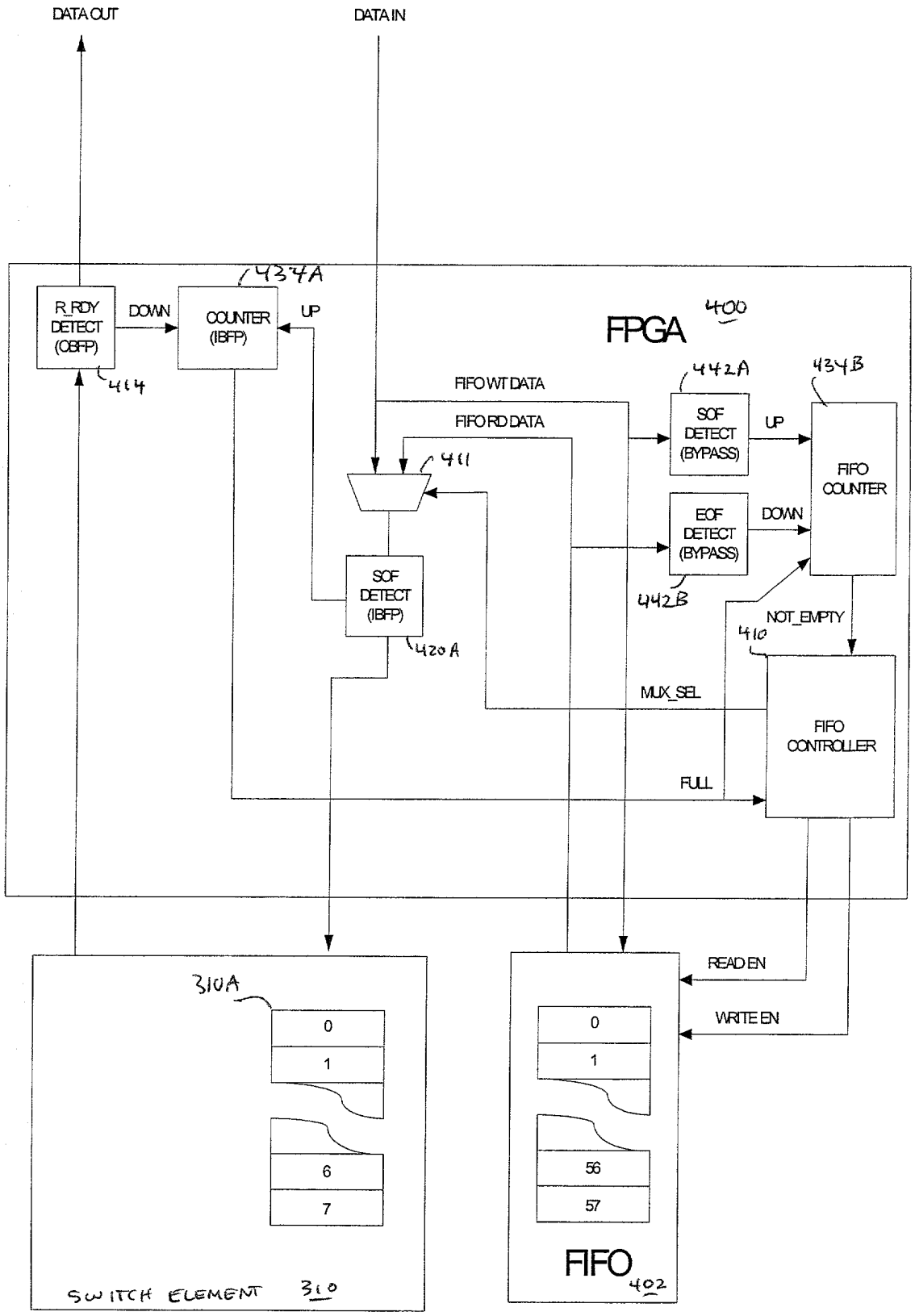
DATA OUT
DATA IN
FPGA
400
R_RDY DETECT (OBFP)
DOWN
COUNTER (IBFP)
UP
434A
414
FIFO WT DATA
FIFO RD DATA
411
SOF DETECT (BYPASS)
442A
UP
434B
FIFO COUNTER
EOF DETECT (BYPASS)
DOWN
442B
SOF DETECT (IBFP)
420A
NOT_EMPTY
410
MUX_SEL
FIFO CONTROLLER
FULL
READ EN
WRITE EN
310A
0
1
6
7
SWITCH ELEMENT 310
0
1
56
57
FIFO 402

FIG. 12

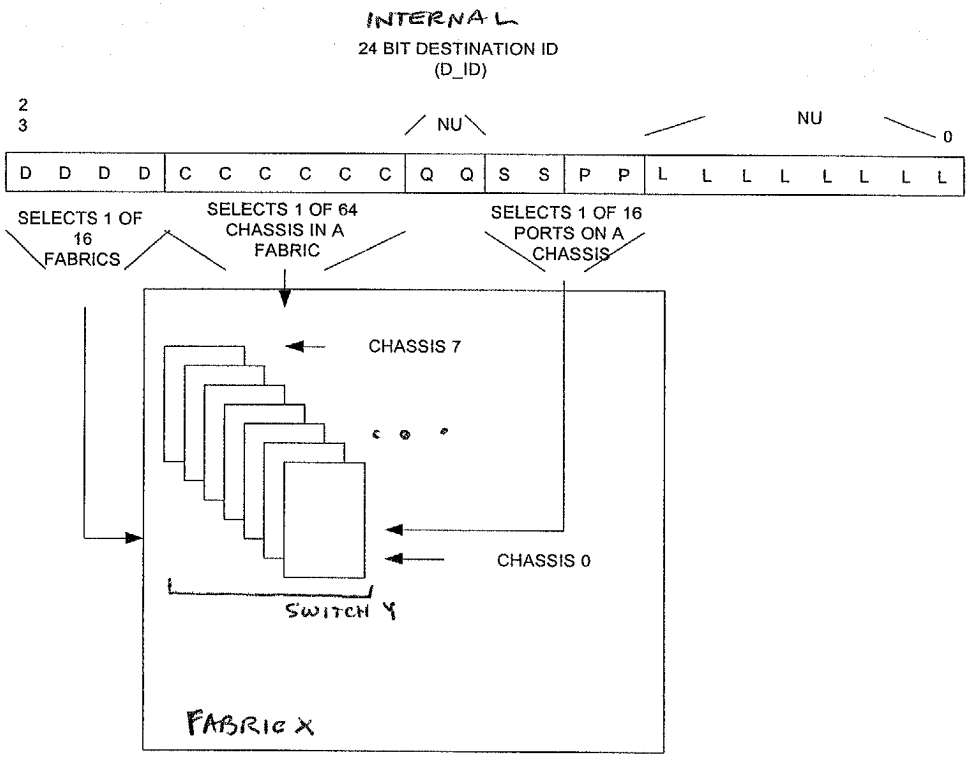

FIG. 13

Docket/App No.: 2997.1005-001
Title: Fibre Channel Address Adaptor Having Data Buffer Extension...
Inventors: Steven G. Schmidt *et al.*

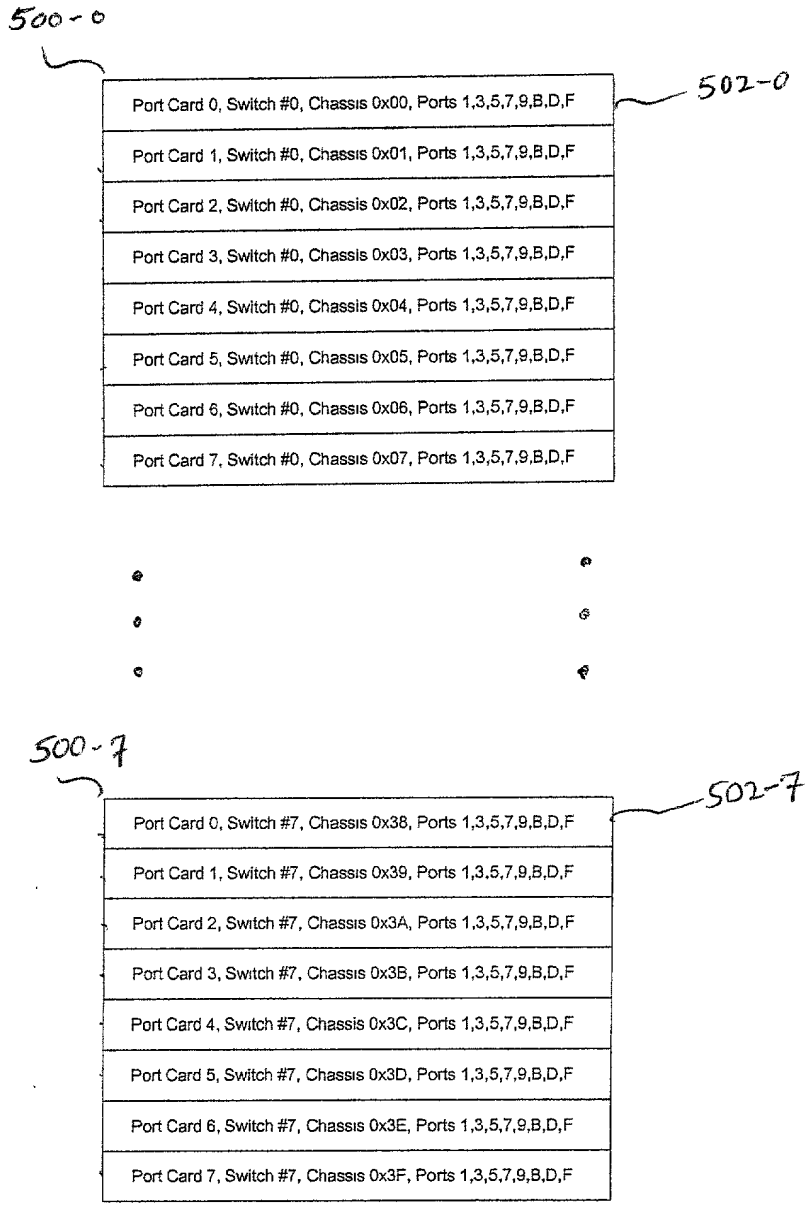
500-0
Port Card 0, Switch #0, Chassis 0x00, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #0, Chassis 0x01, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #0, Chassis 0x02, Ports 1,3,5,7,9,B,D,F
Port Card 3, Switch #0, Chassis 0x03, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #0, Chassis 0x04, Ports 1,3,5,7,9,B,D,F
Port Card 5, Switch #0, Chassis 0x05, Ports 1,3,5,7,9,B,D,F
Port Card 6, Switch #0, Chassis 0x06, Ports 1,3,5,7,9,B,D,F
Port Card 7, Switch #0, Chassis 0x07, Ports 1,3,5,7,9,B,D,F
502-0
500-7
Port Card 0, Switch #7, Chassis 0x38, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #7, Chassis 0x39, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #7, Chassis 0x3A, Ports 1,3,5,7,9,B,D,F
Port Card 3, Switch #7, Chassis 0x3B, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #7, Chassis 0x3C, Ports 1,3,5,7,9,B,D,F
Port Card 5, Switch #7, Chassis 0x3D, Ports 1,3,5,7,9,B,D,F
Port Card 6, Switch #7, Chassis 0x3E, Ports 1,3,5,7,9,B,D,F
Port Card 7, Switch #7, Chassis 0x3F, Ports 1,3,5,7,9,B,D,F
502-7

FIG. 14

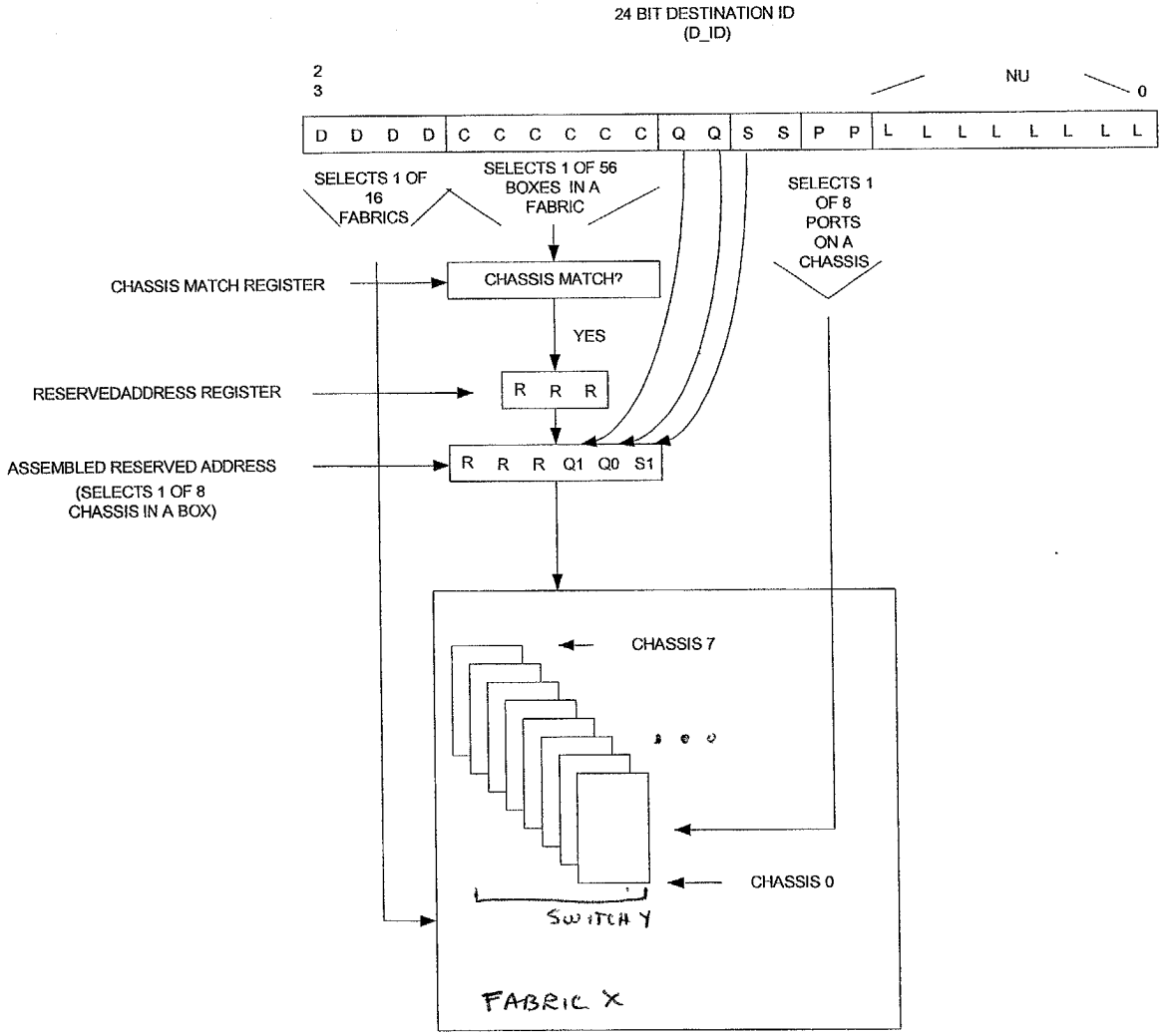

FIG. 15

Docket/App No.: 2997.1005-001
Title: Fibre Channel Address Adaptor Having Data Buffer Extension...
Inventors: Steven G. Schmidt *et al.*

600-0

602-0

Port Card 0, Switch #0, Chassis 0x00, Ports 0,1,2,3,4,5,6,7
Port Card 1, Switch #0, Chassis 0x00, Ports 8,9,A,B,C,D,E,F
Port Card 2, Switch #0, Chassis 0x00, Ports 10,11,12,13,14,15,16,17
Port Card 3, Switch #0, Chassis 0x00, Ports 18,19,1A,1B,1C,1D,1E,1F
Port Card 4, Switch #0, Chassis 0x00, Ports 20,21,22,23,24,25,26,27
Port Card 5, Switch #0, Chassis 0x00, Ports 28,29,2A,2B,2C,2D,2E,2F
Port Card 6, Switch #0, Chassis 0x00, Ports 30,31,32,33,34,35,36,37
Port Card 7, Switch #0, Chassis 0x00, Ports 38,39,3A,3B,3C,3D,3E,3F

⋮ ⋮

600-55

602-55

Port Card 0, Switch #55, Chassis 0x37, Ports 0,1,2,3,4,5,6,7
Port Card 1, Switch #55, Chassis 0x37, Ports 8,9,A,B,C,D,E,F
Port Card 2, Switch #55, Chassis 0x37, Ports 10,11,12,13,14,15,16,17
Port Card 3, Switch #55, Chassis 0x37, Ports 18,19,1A,1B,1C,1D,1E,1F
Port Card 4, Switch #55, Chassis 0x37, Ports 20,21,22,23,24,25,26,27
Port Card 5, Switch #55 Chassis 0x37, Ports 28,29,2A,2B,2C,2D,2E,2F
Port Card 6, Switch #55, Chassis 0x37, Ports 30,31,32,33,34,35,36,37
Port Card 7, Switch #55, Chassis 0x37, Ports 38,39,3A,3B,3C,3D,3E,3F

FIG. 16

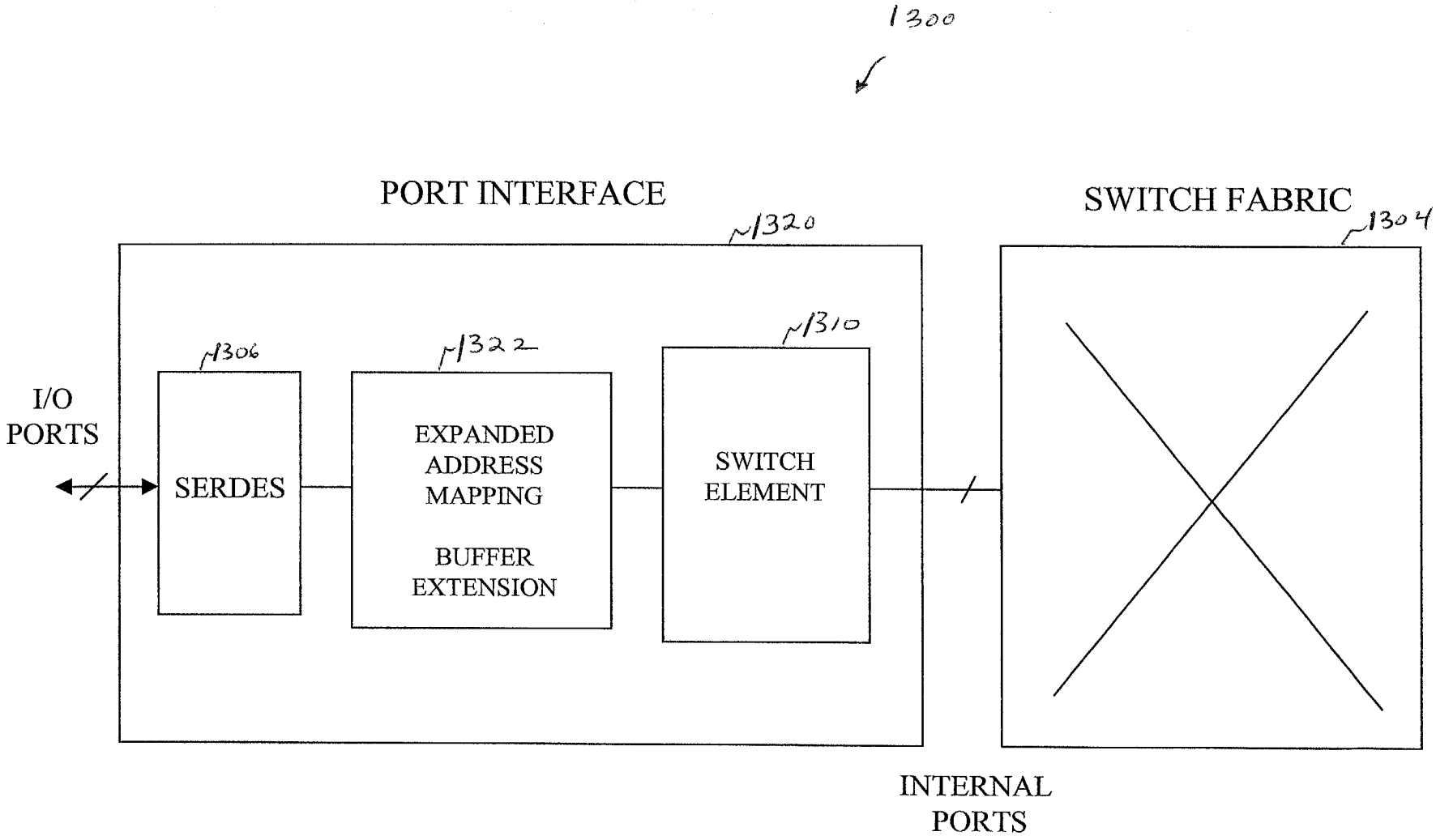

FIG. 17

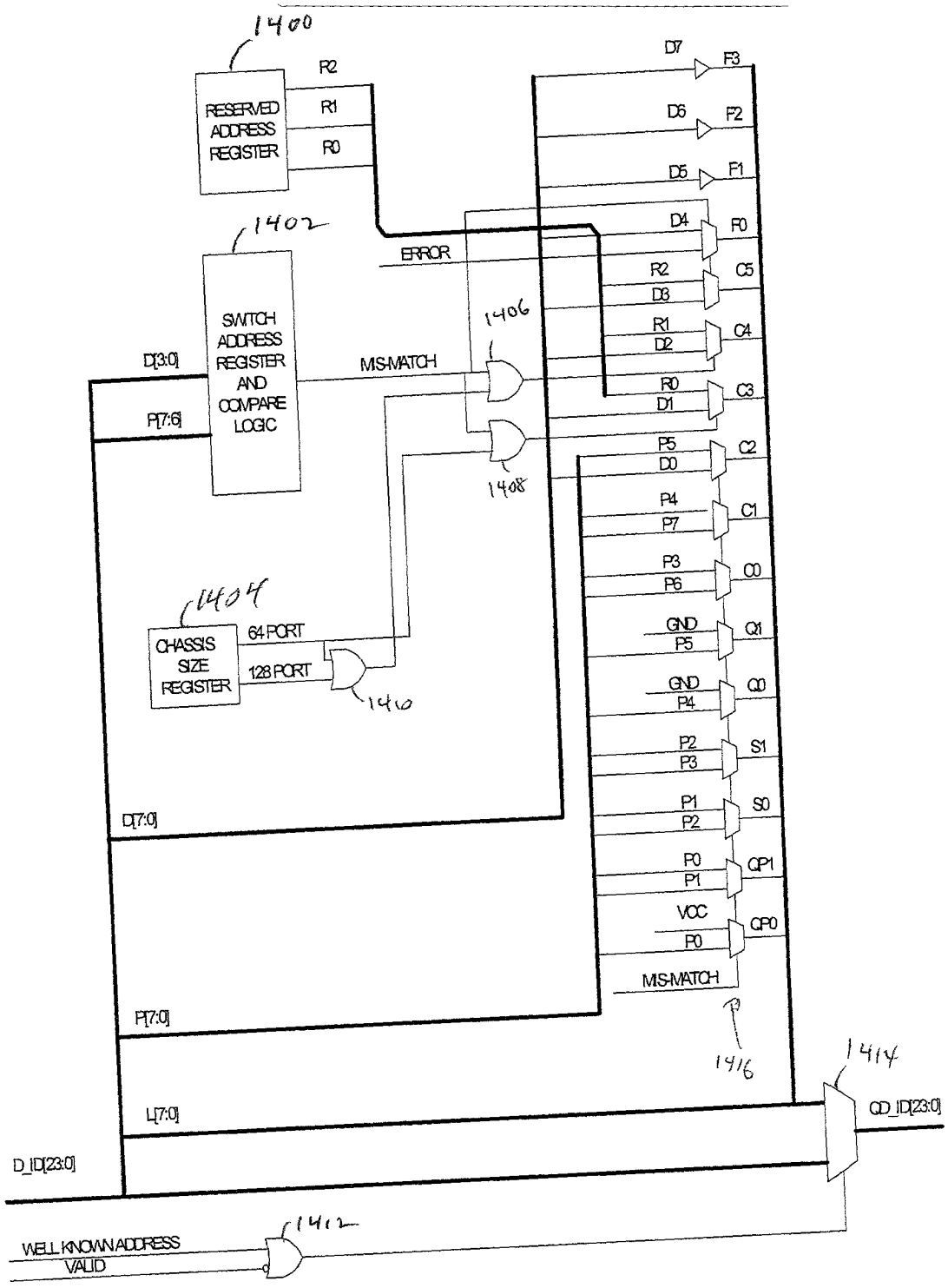

FIG. 18

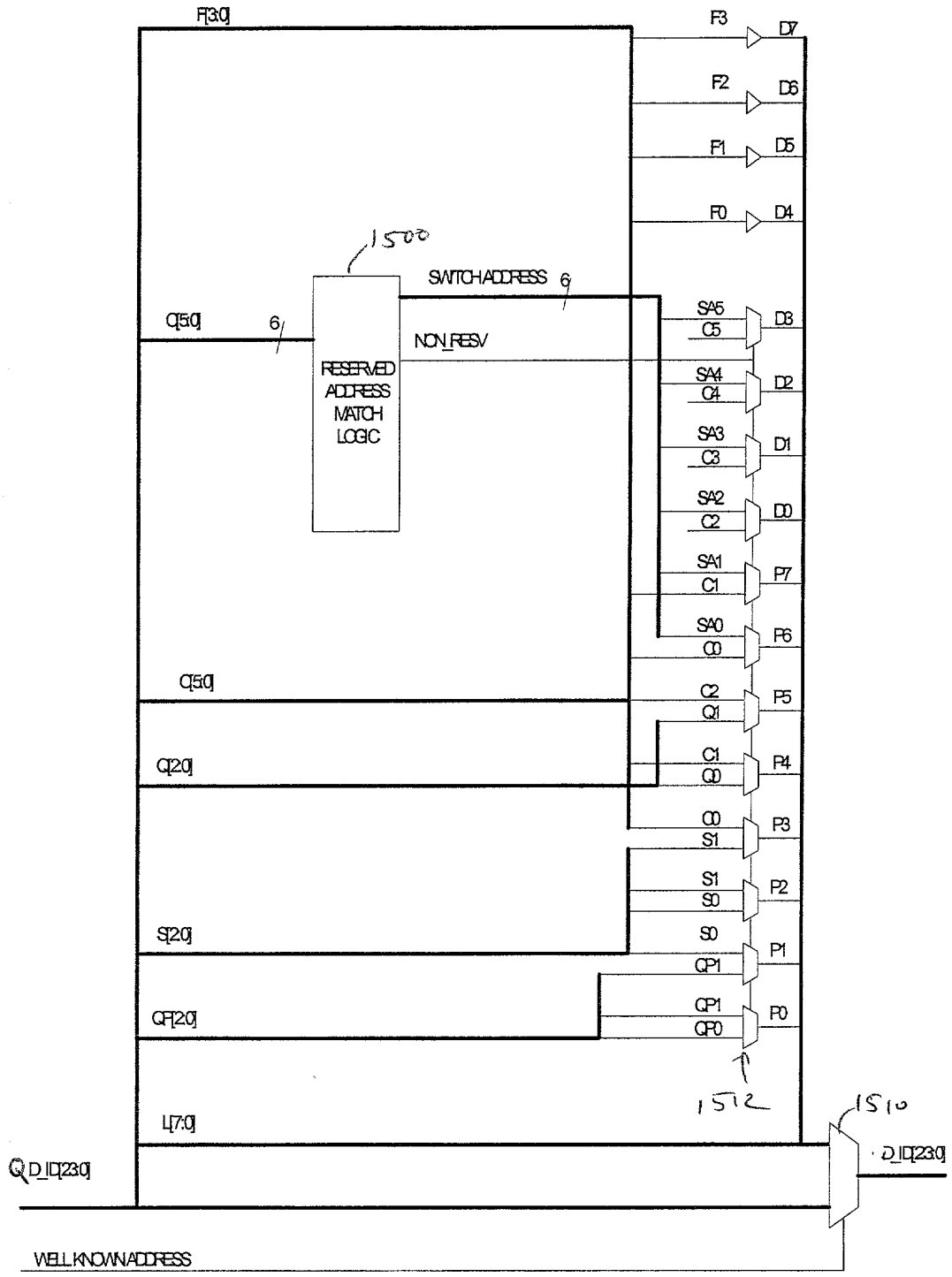
F[3:0]
F3
D7
F2
D6
F1
D5
F0
D4
1500
SWITCHADDRESS
6
Q[5:0]
6
NON_RESV
RESERVED ADDRESS MATCH LOGIC
SA5
C5
D3
SA4
C4
D2
SA3
C3
D1
SA2
C2
D0
SA1
C1
P7
SA0
C0
P6
Q[5:0]
C2
Q1
P5
Q[2:0]
C1
Q0
P4
C0
S1
P3
S1
S0
P2
S[2:0]
S0
QP1
P1
QP[2:0]
QP1
QP0
P0
1512
1510
L[7:0]
Q D_ID[23:0]
D_ID[23:0]
WELL KNOWN ADDRESS

FIG. 19

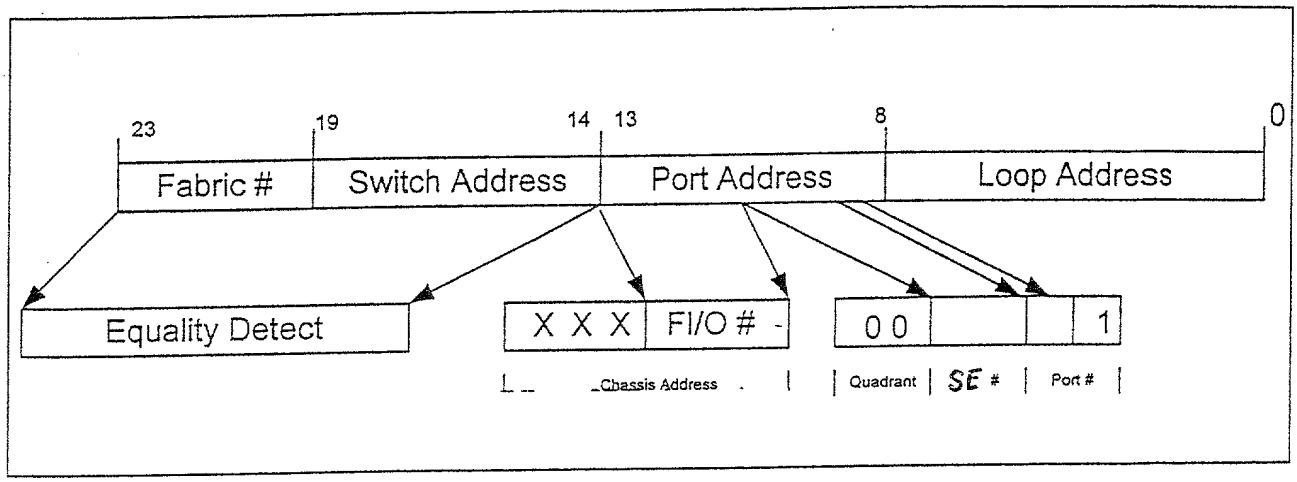

FIG. 20

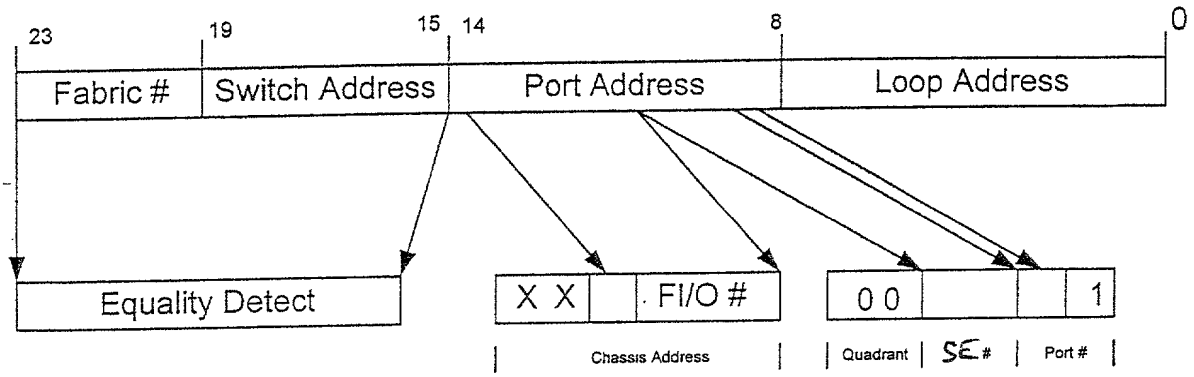
23
19
15
14
8
0
Fabric #
Switch Address
Port Address
Loop Address
Equality Detect
X X
FI/O #
0 0
1
Chassis Address
Quadrant
SE#
Port #

FIG. 21

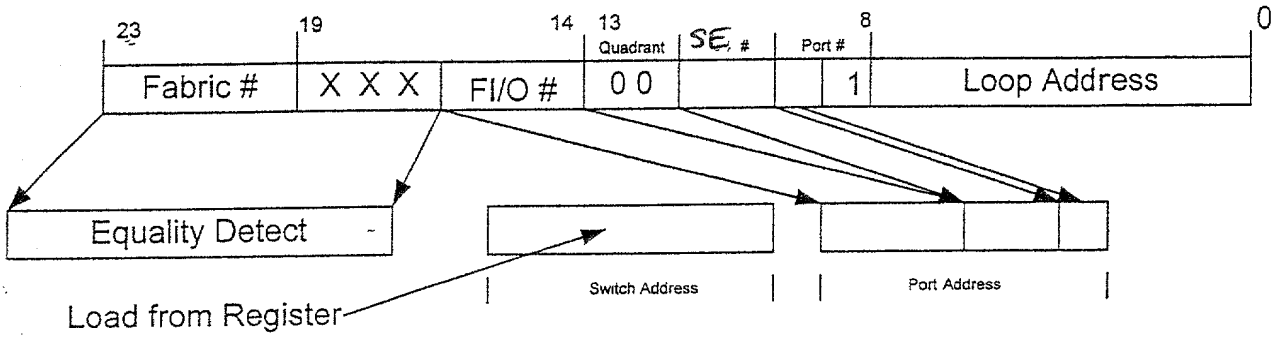
23
19
14
13
Quadrant
SE #
Port #
8
0
Fabric #
X X X
FI/O #
0 0
1
Loop Address
Equality Detect
Load from Register
Switch Address
Port Address

FIG. 22

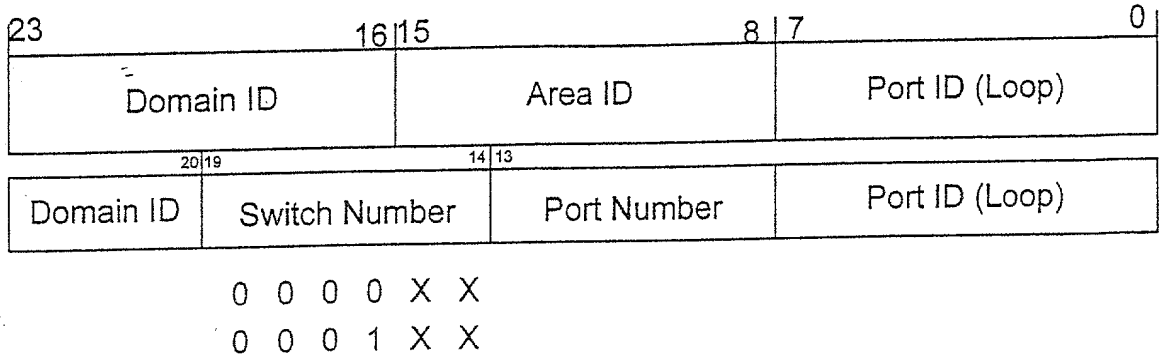
23
16
15
8
7
0
Domain ID
Area ID
Port ID (Loop)
20
19
14
13
Domain ID
Switch Number
Port Number
Port ID (Loop)
0 0 0 0 X X
0 0 0 1 X X

FIG. 23